High-Sensitivity "Super HAD CCD II" Security Camera Image Sensors
ICX632AKA/ICX633AKA Diagonal 6.0 mm (Type 1/3) 250K/290K Effective Pixels
ICX648AKA/ICX649AKA Diagonal 4.5 mm (Type 1/4) 380K/440K Effective Pixels

The Type 1/3 and Type 1/4 CCDs have both become mainstream optical systems in the security camera market, where superb imaging characteristics are required.
Compared to Sony's existing ICX404AK/ICX405AK*1 and ICX228AK/ICX229AK*2 products, the ICX632AKA/ICX633AKA and ICX648AKA/ICX649AKA of this release feature significantly improved sensitivity achieved through improved condensing and optimized spectral sensitivity characteristics.
The ICX632AKA/ICX633AKA also feature improved ease of use, since in addition to the earlier 5.0 V, they also support the use of 3.3 V for both the horizontal transfer clock voltage and the reset gate clock voltage.
*1 **See CX-News Vol. 23** *2 **See CX-News Vol. 20**

ICX632AKA: Diagonal 6.0 mm (Type 1/3), NTSC, 250K pixels

ICX633AKA: Diagonal 6.0 mm (Type 1/3), PAL, 290K pixels

ICX648AKA: Diagonal 4.5 mm (Type 1/4), NTSC, 380K pixels

ICX649AKA: Diagonal 4.5 mm (Type 1/4), PAL, 440K pixels

- High sensitivity (+7 dB over existing Sony products), new spectral sensitivity characteristics
- Support for reduced drive voltage amplitudes (3.3 V typical)
- Compatibility with existing Sony products

*: "Super HAD CCD" and *Super* **HAD CCD** are registered trademarks of Sony Corporation.

The ICX632AKA/ICX633AKA and ICX648AKA/ICX649AKA are color CCD image sensors mainly designed for security camera applications. These devices feature improved characteristics compared to the existing Sony ICX404AK/ICX405AK and ICX228AK/ICX229AK.
While the saturation signal and smear level performance has been maintained in the ICX632AKA/ICX633AKA and improved in the ICX648AKA/ICX649AKA, Sony has significantly improved the sensitivity, which is critical for security camera applications.

High Sensitivity and New Spectral Sensitivity Characteristics

The ICX632AKA/ICX633AKA and ICX648AKA/ICX649AKA of this release provide a significantly improved focusing of light onto the photodiodes due to an increased aperture ratio and an improved upper section structure. (See figure 1.)
Also, by adopting new complementary color pigments in the color filters, Sony increased the sensitivity to the blue end of the spectrum (shorter wavelengths) and achieved well-balanced spectral sensitivity characteristics. (See figure 2.)
The combination of these technological improvements results in a significant increase in the sensitivity characteristics that totals + 7 dB. Compared to the existing ICX228AK/ICX229AK, the adoption of these new color filters achieves a significant improvement in light resistance as well. As a result, these devices are resistant to color filter fading when subjected to bright light for extended periods, and are thus are also appropriate for use in outdoor applications.

Support for Reduced Amplitude Drive Voltage

The ICX632AKA/ICX633AKA support not only the same 5.0 V (typical) level used in existing products but also a 3.3 V (typical) level for both the horizontal transfer clock voltage and the reset gate clock voltage. This can have a large effect in reducing power consumption by using a common power supply for both the image sensors and peripheral circuits.

Compatibility with Existing Sony Products

In these new products, Sony has achieved compatibility by making the image size, pixel count, drive timing, package, and pin assignment the same as in existing products (the ICX404AK/ICX405AK and ICX228AK/ICX229AK). The ICX632AKA/ICX633AKA feature improved reset gate drive and, compared to the existing ICX404AK/ICX405AK, allow a reduction in the number of components in the external drive circuit.
Furthermore, the ICX648AKA/ICX649AKA use 12 V as the supply voltage and -5 V as the vertical clock bias and as a result achieve the same low power (118 mW) as the existing products.

V O I C E

The security camera market has been expanding rapidly in recent years and CCD devices that have evolved proportionally to this growth are strongly desired. To respond to these needs, we developed these CCD products which achieve higher sensitivity and lower power consumption. I hope that improved security camera performance due to these improved characteristics will lead to reduced crime. I strongly recommend these CCDs, which achieve the industry's highest level of image sensor sensitivity.

Figure 1 "Super HAD CCD II" Structure

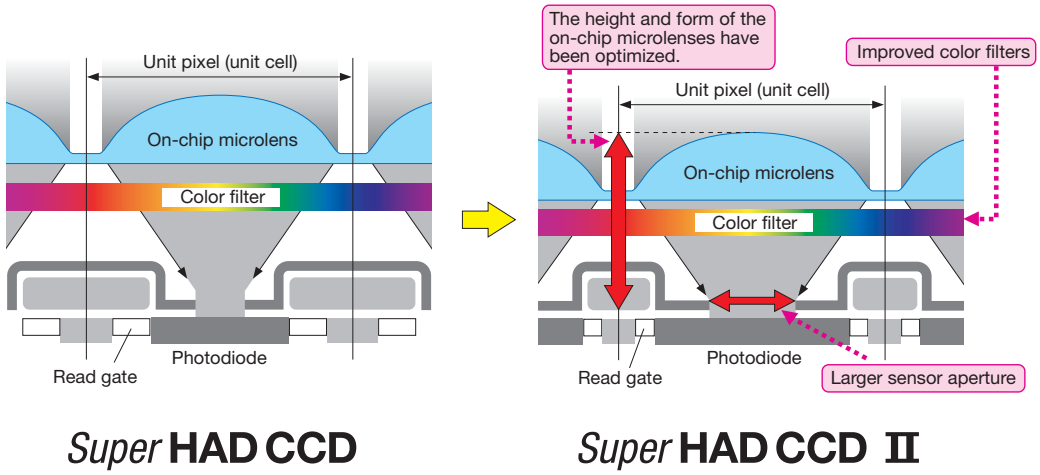


Figure 2 Spectral Sensitivity Characteristics Comparison

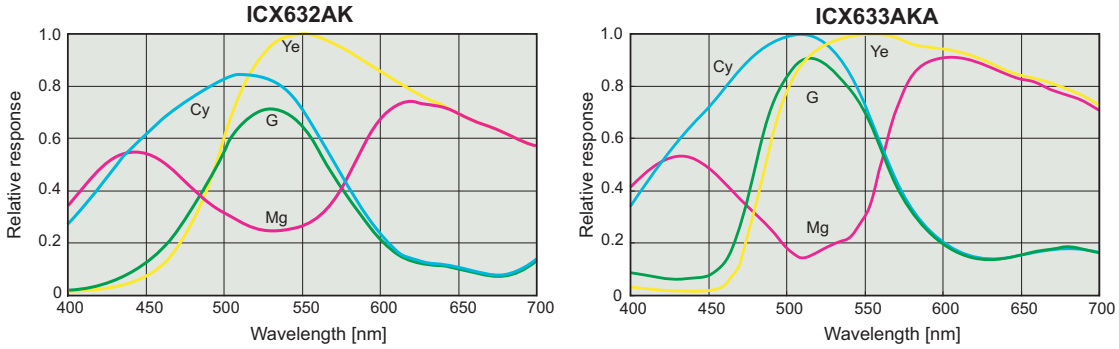


Table 1 Device Structure

Item		ICX632AKA	ICX633AKA	ICX648AKA	ICX649AKA
Image size		Diagonal 6.0 mm (Type 1/3)	←	Diagonal 4.5 mm (Type 1/4)	←
TV format		NTSC	PAL	NTSC	PAL
Transfer method		Interline transfer method	←	←	←
Total number of pixels		Approx. 270K pixels (537H x 505V)	Approx. 320K pixels (537H × 597V)	Approx. 410K pixels (811H × 508V)	Approx. 470K pixels (795H × 596V)
Number of effective pixels		Approx. 250K pixels (510H x 492V)	Approx. 290K pixels (500H × 582V)	Approx. 380K pixels (768H × 494V)	Approx. 440K pixels (752H × 582V)
Chip size (H) × (V)		5.59 mm×4.68 mm	←	4.34 mm×3.69 mm	←
Unit cell size (H) × (V)		9.60 µm×7.50 µm	9.80 µm×6.30µm	4.75 µm×5.55 µm	4.85 µm×4.65 µm
Optical blacks	Horizontal	Front: 2 pixels, rear: 25 pixels	Front: 7 pixels, rear: 30 pixels	Front: 3 pixels, rear: 40 pixels	Front: 3 pixels, rear: 40 pixels
	Vertical	Front: 12 pixels, rear: 1 pixel	Front: 14 pixels, rear: 1 pixel	Front: 12 pixels, rear: 2 pixels	Front: 12 pixels, rear: 2 pixels
Number of dummy bits		Horizontal: 16 Vertical: 1 (Only in even fields)	←	Horizontal: 22 Vertical: 1 (Only in even fields)	←
Horizontal drive frequency		9.54562 MHz	9.4581 MHz	14.3182 MHz	14.1875 MHz
Package		16-pin DIP (Plastic)	←	14-pin DIP (Plastic)	←
Supply voltages VDD/VL (typical values)		15 V / –7 V	←	12 V / –5 V	←

Table 2 Imaging Characteristics

Item		ICX404AK ICX405AK	ICX632AKA ICX633AKA	ICX228AK ICX229AK	ICX648AKA ICX649AKA	Remarks
Sensitivity (F5.6)	Typ.	1700mV	3800mV	450mV 440mV	1050mV 950mV	3200K, 706cd/m^2
Saturation signal	Min.	1000mV	←	800mV 720mV	1000mV	Ta = 60°C
Smear (F5.6)	Typ.	–115dB	←	–100dB	–105dB	V/10 method

SONY

CXD3142R

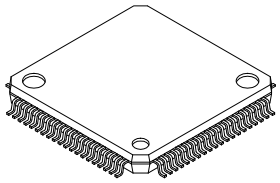
Signal Processor LSI for Single-Chip CCD Color Camera

Description

The CXD3142R is a signal processor LSI for Ye, Cy, Mg and G single-chip CCD color cameras. In addition to basic camera signal processing functions, it includes an AE/AWB detection circuit, a sync signal generation circuit and an external sync circuit, etc.

This chip also has a built-in microcontroller to realize basic camera functions such as AE/AWB without an external microcomputer.

80 pin LQFP (Plastic)



Features

- Generates timing pulses to drive the 510H CCD image sensor
  - Sync signal generation function
  - Luminance/chroma signal processing
  - Luminance/chroma signal integral detector
  - Automatically control camera function
- Supports NTSC/PAL modes
- Supports 510H system CCD image sensor
- Built-in 9-bit A/D converter
- Analog composite output
  - — Built-in digital encoder
  - — 10-bit D/A converter output
- Digital output
  - — YUV 8-bit multiplex output
- Supports external sync functions
- AE/AWB detector
- Block control functions with a built-in microcontroller
  - — AE/AWB/YC/CLAMP/SG control functions
- Peripheral IC communication control functions
  - — EVR, EEPROM communication control
- Serial communication function
  - — Microcomputer (3 wires)

Absolute Maximum Ratings

• Supply voltage	V_{DD}	V_{SS} – 0.5 to +4.6	V
	AV_{DD}	V_{SS} – 0.5 to +4.6	V
• Input voltage	V_I	V_{SS} – 0.5 to V_{DD} + 0.5	V
• Output voltage	V_O	V_{SS} – 0.5 to V_{DD} + 0.5	V
• Operating temperature			
	Topr	–20 to + 75	°C
• Storage temperature			
	Tstg	–55 to +150	°C

Recommended Operating Conditions

• Supply voltage	V_{DD}	3.0 to 3.6	V
	AV_{DD} (AVD1, 2, 5, 6)	3.0 to 3.6	V
	AV_{DD} (AVD4)	3.0 to 5.5	V
• Operating temperature			
	Topr	–20 to +75	°C

Applications

- Industrial CCD cameras
  (surveillance/FA/image input cameras)
- Multimedia CCD cameras
  (teleconferencing/personal computer cameras)

Applicable CCD Image Sensors*

510H color CCDs (Type 1/3, 1/4, 1/6 NTSC/PAL)

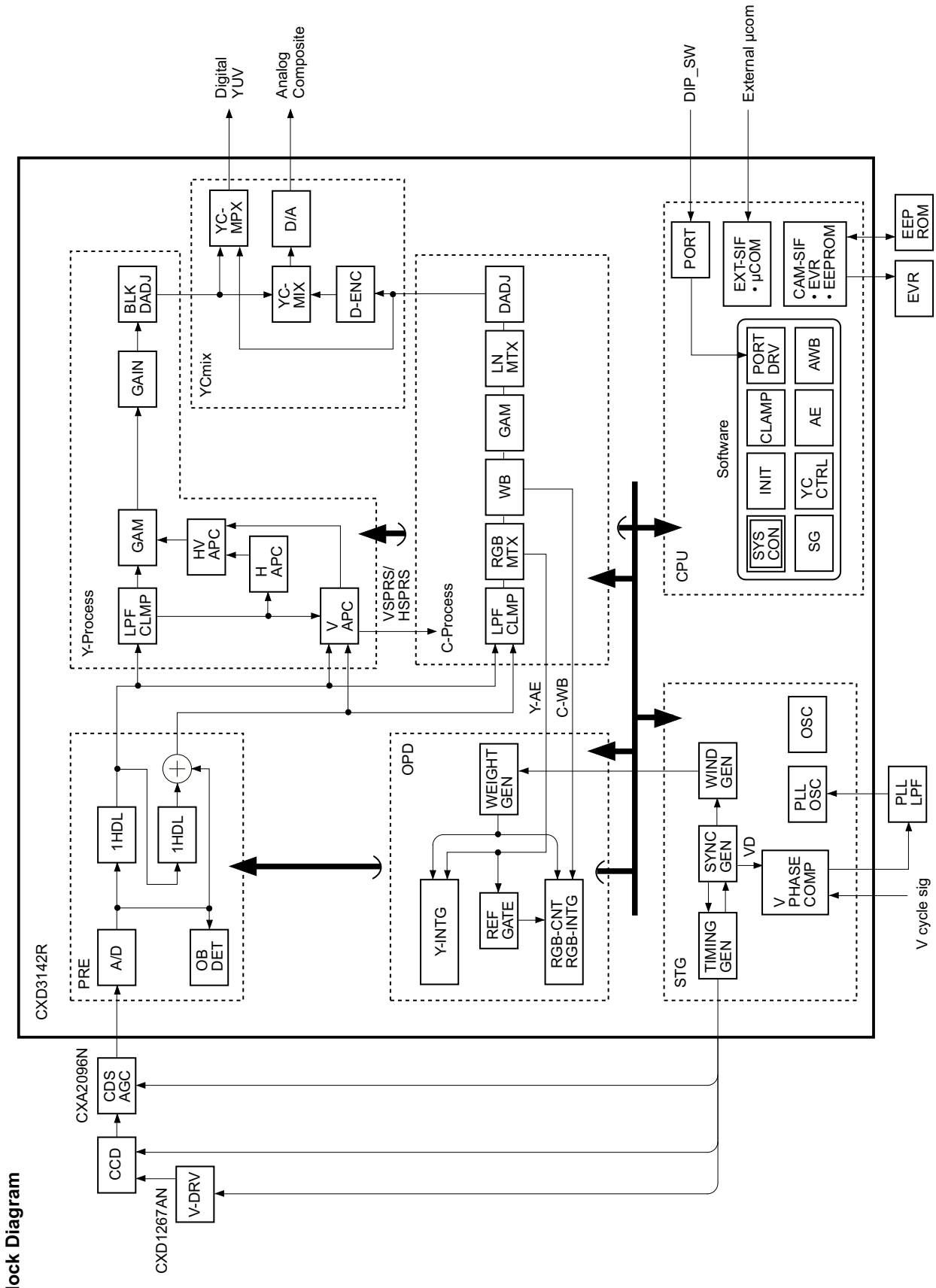
Supported Relates LSIs

V-Driver: CXD1267AN
AGC: CXA2096N
EVR: MB88347 (Fujitsu Limited.)
EEPROM: CAT64LC40JI
(Catalyst Semiconductor Inc.)
AK6420
(Asahi Kasei Microsystems Co.,Ltd.)

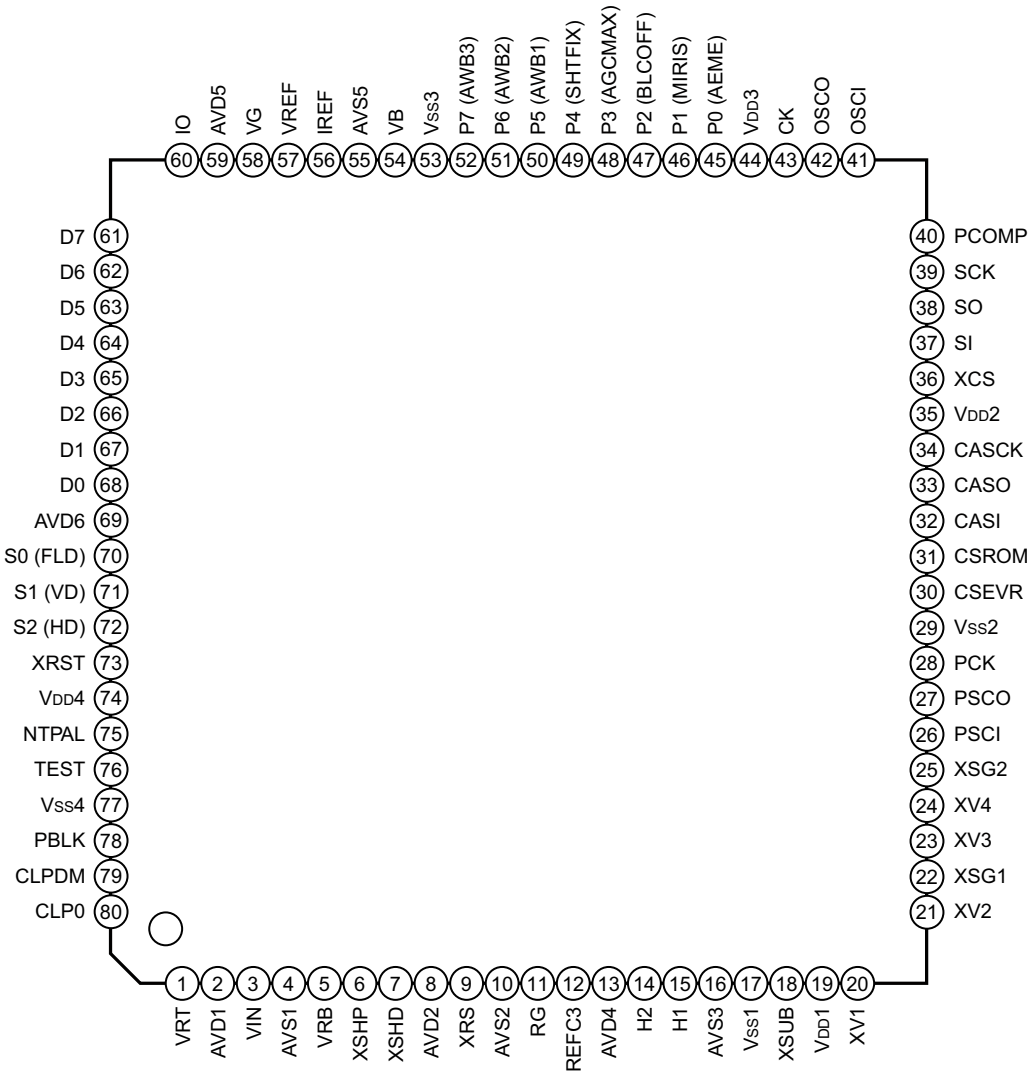
* Applicable CCD Image Sensors are applicable products as of preparing this data sheet.
They may be changed according to the version up and production stop of CCD image sensor.

E02523-PS

Block Diagram



Pin Configuration



Note) Symbols in parentheses are the signal names when the LSI is switched by the serial communication settings.

All pin symbols (pin names) for the CXD3142R are the names next to the pin No. (outside the parentheses).

Pin Description

Pin No.	Symbol	I/O	Description		Power supply
1	VRT	I (A)	A/D converter reference voltage (top) input.	A/D	AVD1
2	AVD1	—	Power supply for A/D converter. (+3.3V)		
3	VIN	I (A)	A/D converter analog signal input.		
4	AVS1	—	GND		
5	VRB	I (A)	A/D converter reference voltage (bottom) input.		
6	XSHP	O	Precharge level sample-and-hold pulse output.	S/H	AVD2
7	XSHD	O	Data sample-and-hold pulse output.		
8	AVD2	—	Power supply for sample-and-hold pulse driver. (+3.3V)		
9	XRS	O	Resampling pulse output.		
10	AVS2	—	GND		
11	RG	O	Reset gate pulse output.	CCD	AVD4
12	REFC3	I	Reference capacitor connection pin.		
13	AVD4	—	Power supply for H driver. (+3.3V/+5.0V)		
14	H2	O	CCD horizontal register transfer pulse output.		
15	H1	O	CCD horizontal register transfer pulse output.		
16	AVS3	—	GND		
17	$V_{SS}1$	—	GND		V_{DD}
18	XSUB	O	CCD electronic shutter pulse output.		
19	$V_{DD}1$	—	Power supply for Logic. (+3.3V)		
20	XV1	O	CCD vertical register transfer pulse output.		
21	XV2	O	CCD vertical register transfer pulse output.		
22	XSG1	O	CCD sensor readout pulse output.		
23	XV3	O	CCD vertical register transfer pulse output.		
24	XV4	O	CCD vertical register transfer pulse output.		
25	XSG2	O	CCD sensor readout pulse output.		
26	PSCI	I	Oscillation cell input. (slave)	OSC2	
27	PSCO	O	Oscillation cell output. (slave)		
28	PCK	I	System clock input. (slave)		
29	$V_{SS}2$	—	GND		
30	CSEVR	O	Chip select output for camera peripheral ICs. (to EVR)	Peripheral communication	
31	CSROM	O	Chip select output for camera peripheral ICs. (to EEPROM)		
32	CASI	I	Serial data input for camera peripheral ICs. (from EEPROM)		
33	CASO	O	Serial data output for camera peripheral ICs. (to EVR, EEPROM)		
34	CASCK	O	Serial clock output for camera peripheral ICs. (to EVR, EEPROM)		
35	$V_{DD}2$	—	Power supply for Logic. (+3.3V)		

Pin No.	Symbol	I/O	Description		Power supply
36	XCS	I	Chip select input for microcomputer communication.	External communication	V_{DD}
37	SI	I	Serial data input for microcomputer communication.		
38	SO	O	Serial data output for microcomputer communication.		
39	SCK	I	Serial clock input for microcomputer communication.		
40	PCOMP	O/Z	Phase comparator output for PLL.		
41	OSCI	I	Oscillation cell input. (master)	OSC1	
42	OSCO	O	Oscillation cell output. (master)		
43	CK	I	System clock input. (master)		
44	$V_{DD}3$	—	Power supply for Logic. (+3.3V)		
45	P0 (AEME)	I	Port 0 input for mode switch. (AE mode switching)	SW	
46	P1 (MIRIS)	I	Port 1 input for mode switch. (Iris mode switching)		
47	P2 (BL COFF)	I	Port 2 input for mode switch. (Backlight compensation off)		
48	P3 (AGCMAX)	I	Port 3 input for mode switch. (AGC maximum gain switching)		
49	P4 (SHTFIX)	I	Port 4 input for mode switch. (SHUT FIX mode switching)		
50	P5 (AWB1)	I	Port 5 input for mode switch. (AWB mode switching)		
51	P6 (AWB2)	I	Port 6 input for mode switch. (ATW/push lock switching)		
52	P7 (AWB3)	I	Port 7 input for mode switch. (Push lock signal input)		
53	$V_{SS}3$	—	GND		
54	VB	I (A)	Capacitor connection pin. (about 0.1µF)	D/A	AVD5
55	AVS5	—	GND		
56	IREF	O (A)	Reference current setting pin.		
57	VREF	I (A)	Reference voltage setting pin.		
58	VG	I (A)	Capacitor connection pin. (about 0.1µF)		
59	AVD5	—	Power supply for D/A converter. (+3.3V)		
60	IO	O	Composite signal (current) output.		
61	D7	O/Z	Digital signal output.	Digital output	V_{DD}
62	D6	O/Z	Digital signal output.		
63	D5	O/Z	Digital signal output.		
64	D4	O/Z	Digital signal output.		
65	D3	O/Z	Digital signal output.		
66	D2	O/Z	Digital signal output.		
67	D1	O/Z	Digital signal output.		
68	D0	O/Z	Digital signal output.		
69	AVD6	—	Power supply for A/D converter. (+3.3V)		

Pin No.	Symbol	I/O	Description		Power supply
70	S0 (FLD)	O/Z	Sync signal output 0. (FLD signal)	Sync signal	V_{DD}
71	S1 (VD)	O/I/Z	Sync signal output 1. (VD signal)/VD signal input for LL		
72	S2 (HD)	O/Z	Sync signal output 2. (HD signal)		
73	XRST	I	Reset input. (Low: reset, High: normal operation)		
74	$V_{DD}4$	—	Power supply for Logic. (+3.3V)		
75	NTPAL	I	TV mode switching. (Low: NTSC, High: PAL)		
76	TEST	I	Chip test input. Low fixed at normal operation.		
77	$V_{SS}4$	—	GND		
78	PBLK	O	Preblanking pulse output.	S/H	
79	CLPDM	O	Dummy data clamp pulse output.		
80	CLP0	O	Optical black clamp pulse output.		

I: CMOS level input
O: CMOS level output
I/O: Bidirectional input/output
O/Z: Tri-state output
I (A): Analog input
O (A): Analog output
O/I/Z: Bidirectional input/output with Tri-state

Electrical Characteristics

DC Characteristics

(Within recommended operating range)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}1, 2, 3, 4		3.0	3.3	3.6	V
	AVD1, 2, 6		3.0	3.3	3.6	V
	AVD5	D/A output amplitude = 1Vp-p	3.0	3.3	3.6	V
	AVD4		3.0	—	5.5	V
Output voltage	V_{OH}1*1	I_{OH} = 4mA	V_{DD} – 0.4			V
	V_{OL}1*1	I_{OL} = 4mA			0.4	V
	V_{OH}2*2, *6	I_{OH} = 1mA	V_{DD} – 0.4			V
	V_{OL}2*2, *6	I_{OL} = 1mA			0.4	V
Input voltage	V_{T+}*2, *3, *4, *5		0.7V_{DD}			V
	V_{T-}*2, *3, *4, *5				0.2V_{DD}	V
Hysteresis	$V_{T+} – V_{T-}$*2, *3, *5			0.5		V
Input leak current	I_{IH}*7	V_{IN} = V_{DD}	40	100	240	µA

*1 XV1, XV2, XV3, XV4, XSG1, XSG2, XSUB, PBLK, CLPDM, CLP0, SO, CASCK, CASO, CSROM, CSEVR

*2 S1

*3 XRST, XCS, SI, SCK, CASI

*4 NTPAL

*5 P0, P1, P2, P3, P4, P5, P6, P7

*6 S0, S2, D0, D1, D2, D3, D4, D5, D6, D7

*7 TEST

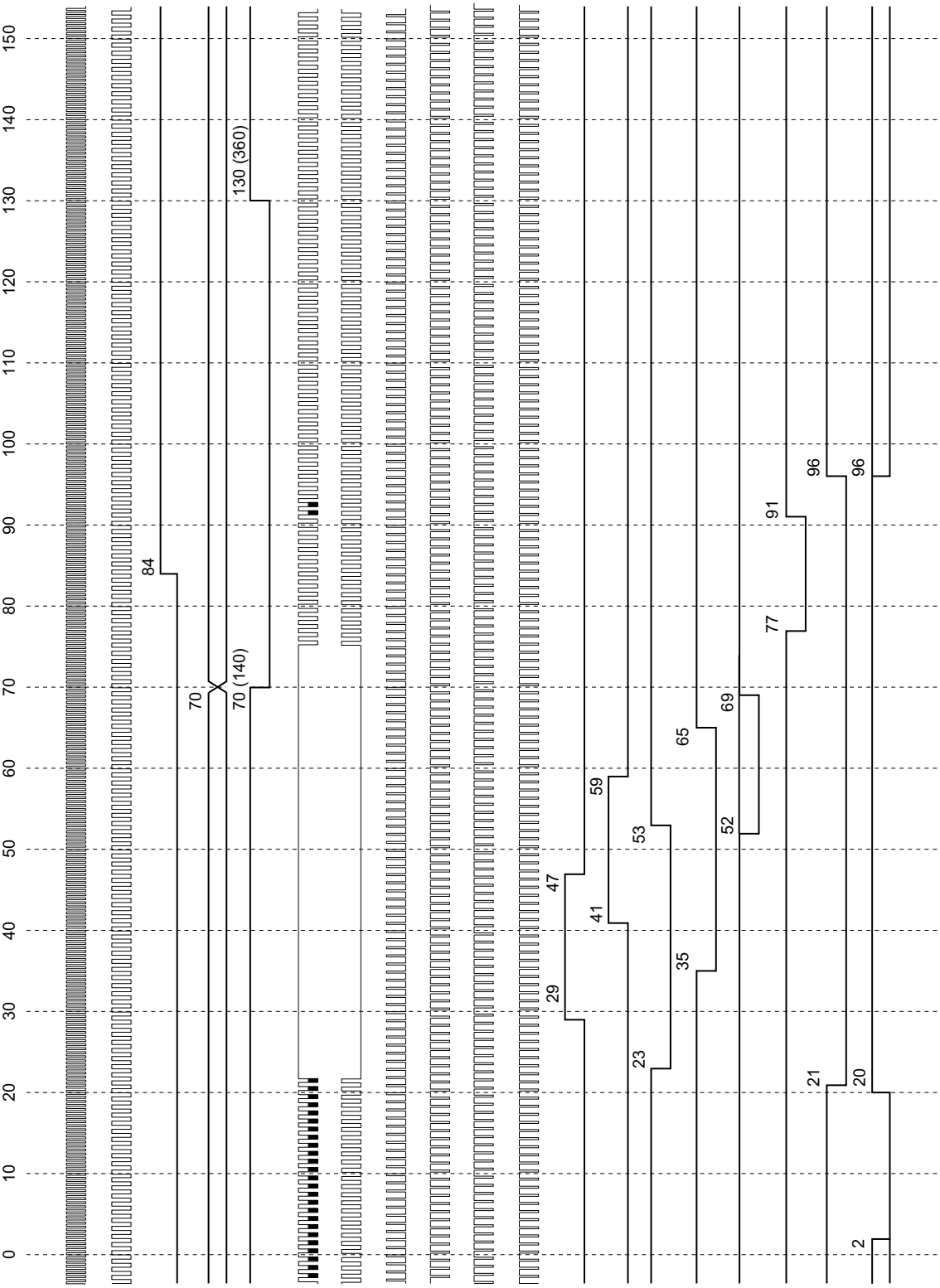
I/O Pin Capacitance

(V_{DD} = V_I = 0V, f = 1MHz)

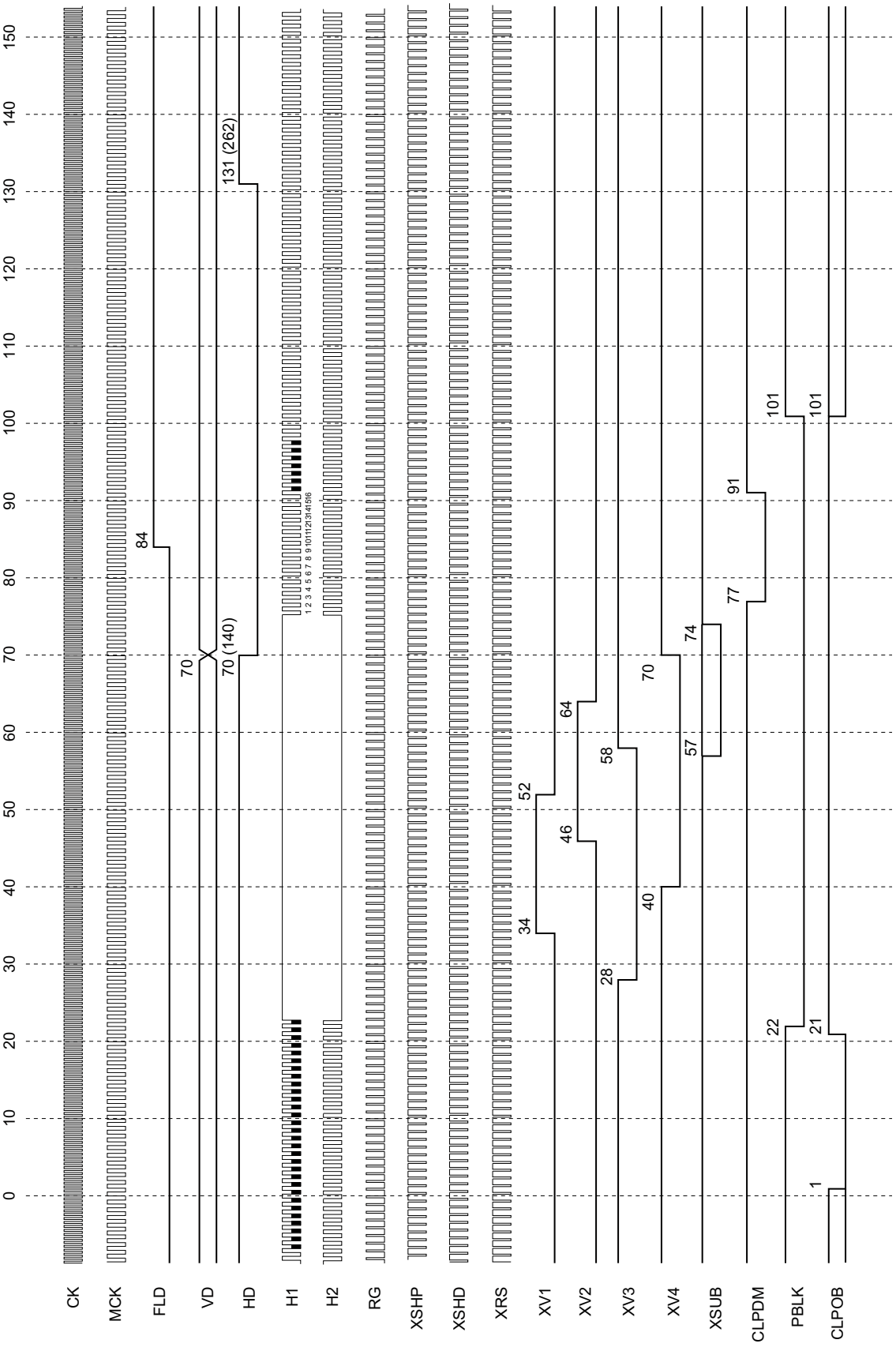
Item	Symbol	Min.	Typ.	Max.	Unit
Input pin capacitance	C_{IN}			9	pF
Output pin capacitance	C_{OUT}			11	pF
I/O pin capacitance	$C_{I/O}$			11	pF

510H NTSC Horizontal Timing Chart

CK: 1212fH (19.06993MHz/52.44ns)
MCK: 606fH (9.53496MHz/104.88ns)

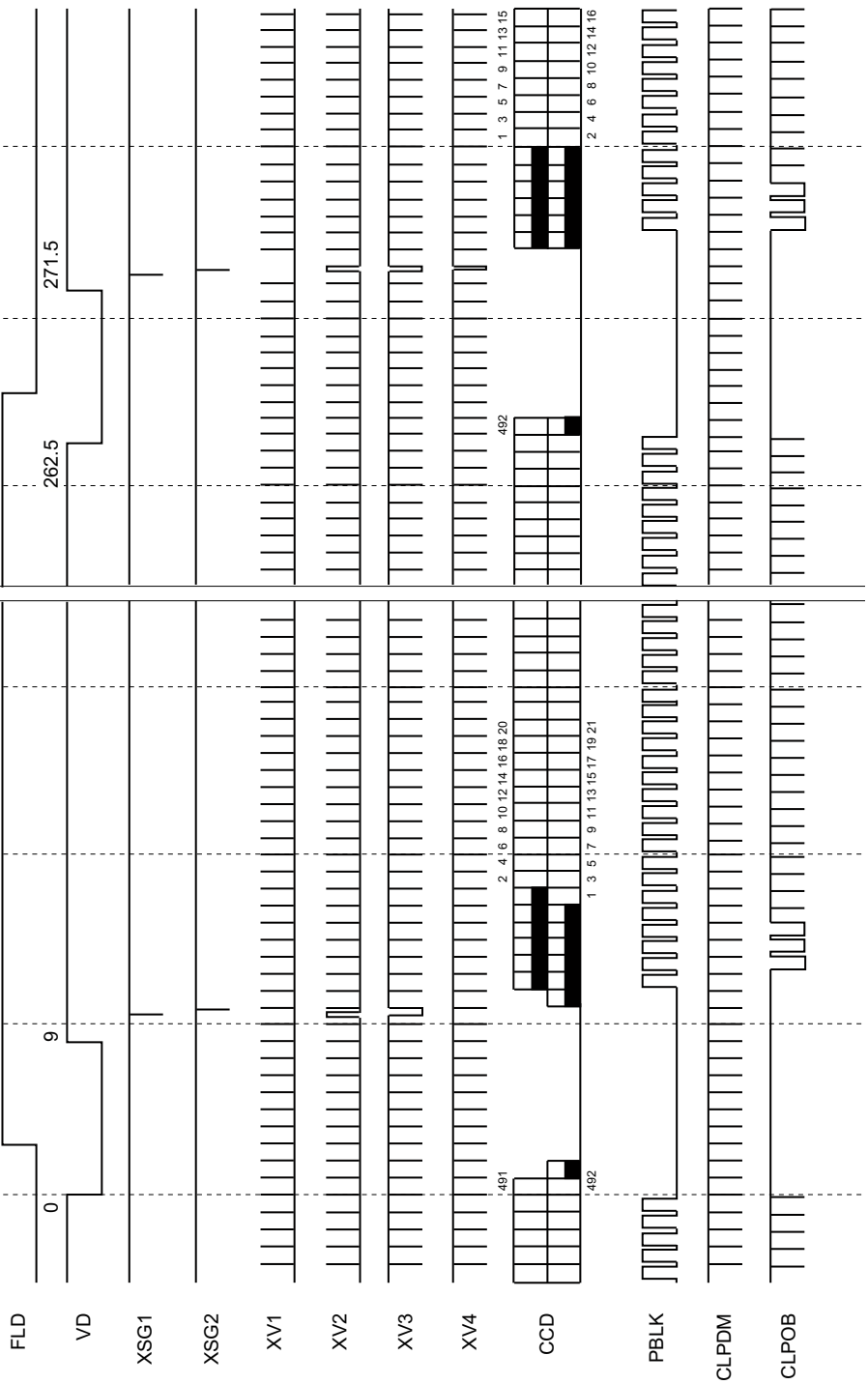


510 PAL Horizontal Timing Chart



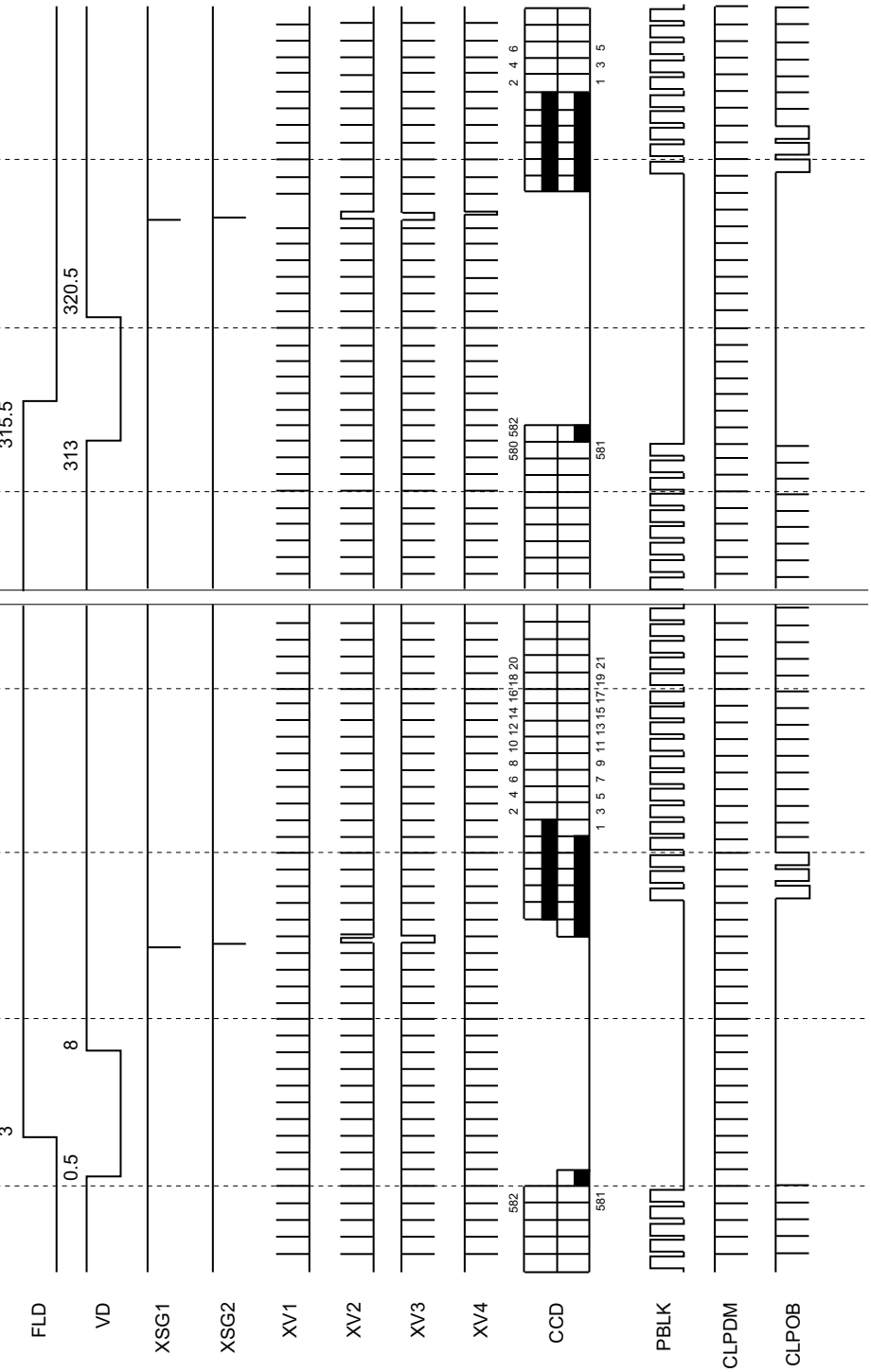
510H NTSC Vertical Timing Chart

CK: 1212fH (19.06993MHz/52.44ns)
MCK: 606fH (9.53496MHz/104.88ns)



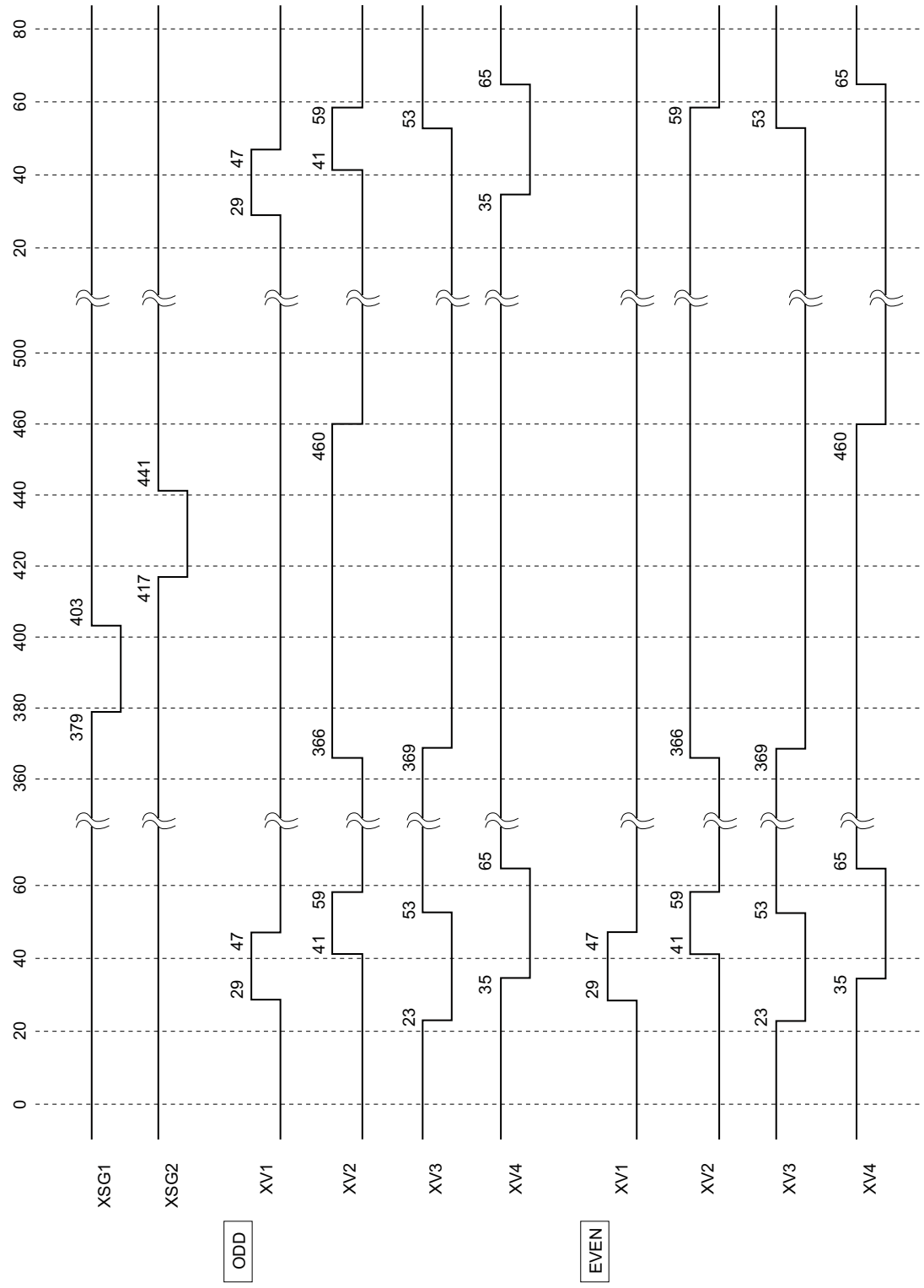
510H PAL Vertical Timing Chart

CK: 1212f_H (18.9375MHz/52.81ns)
MCK: 606f_H (9.46875MHz/105.61ns)



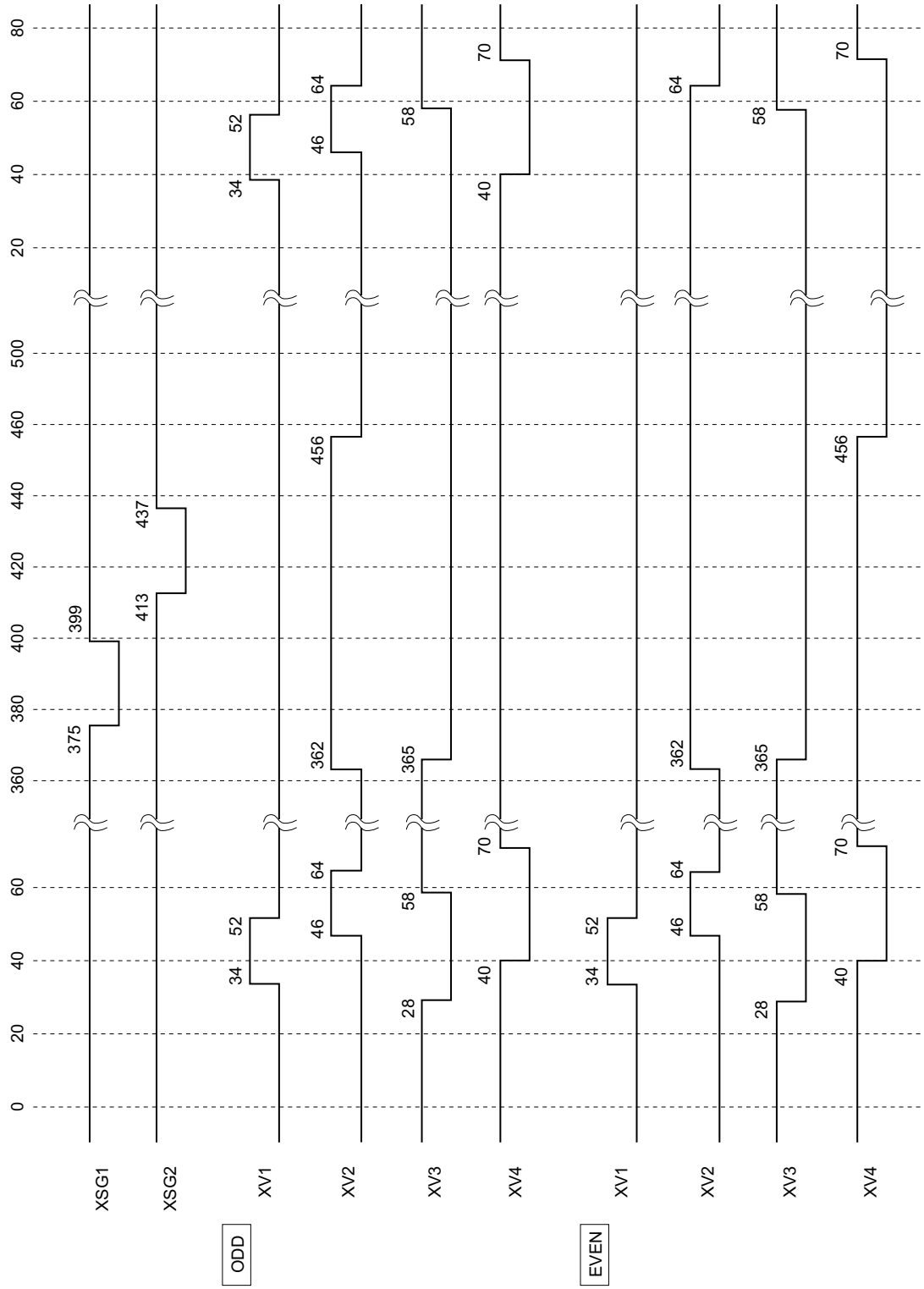
510H NTSC Readout Timing Chart

CK: 1212fH (19.06993MHz/52.44ns)
MCK: 606fH (9.53496MHz/104.88ns)

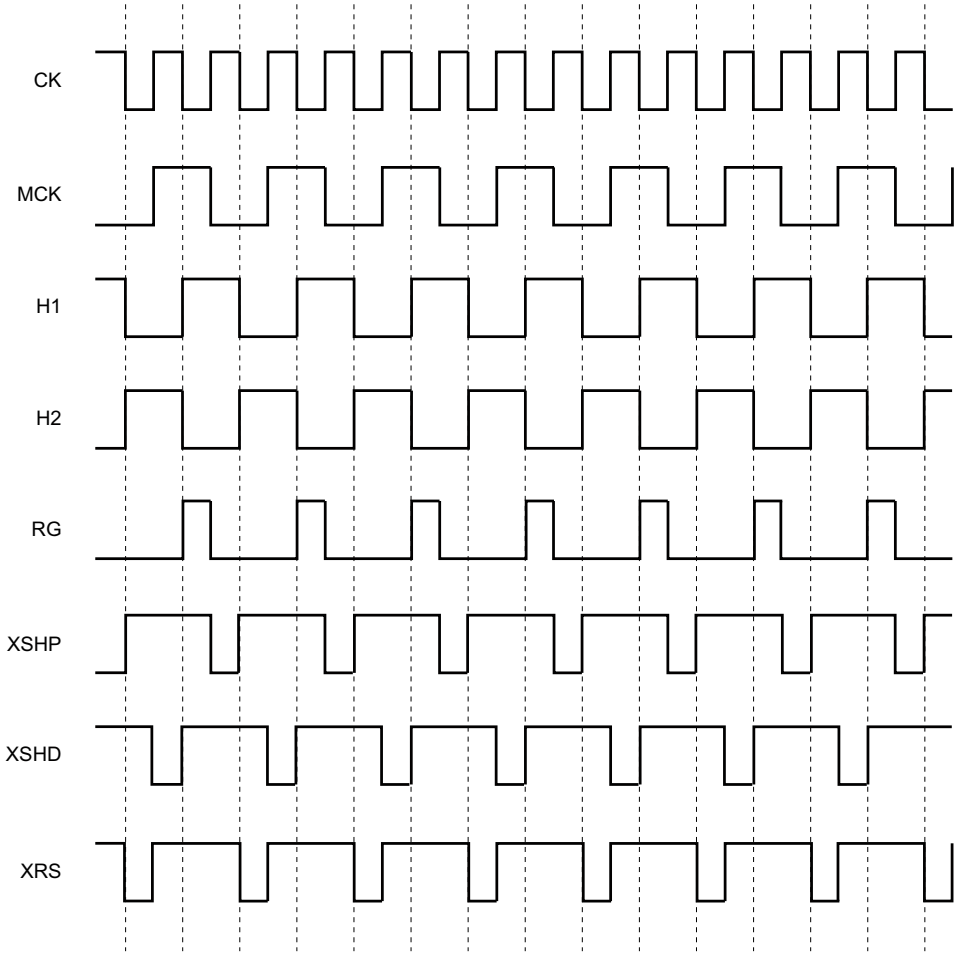


510H PAL Readout Timing Chart

CK: 1212f_H (18.9375MHz/52.81ns)
MCK: 606f_H (9.46875MHz/105.61ns)



510H High-speed Clock Timing chart



Serial Communication Data

Classification of Serial Data

Category		Contents	
	I/O	Byte 0	Byte 1 to
CAT1: SYSCON	I	01h	System configuration
CAT2: CPU	I	02h	CPU configuration
CAT3: PICT	I	03h	Picture parameters
CAT4: AE	I	04h	AE usr specification
CAT5: AWB	I	05h	AWB usr specification
CAT6: ADJUST	I	06h	Adjustment
CAT7: TIMING	I	07h	Timing parameters
CAT8: SOUT	I	08h	Serial OUT setting
	O		Serial OUT data
CAT9: EXTCON	I	09h	External controller

Category 1: SYSCON

CAT1		Serial input				
Byte	bit	Name	Description	#1	Block	Address
0	0	CAT1	LSB Category select code 01h: SYSCON			
	1					
	2					
	3					
	4					
	5					
	6					
	7		MSB			
1	0	NTPAL	NTSC/PAL 0: NTSC, 1: PAL	0	common	01h
	1	OCCF	On-chip color filter 0: Type 1/4, 1: Type 1/3	0	MAIN/C	
	2	(Low)	LSB "0" fixed	0	common	
	3		MSB			
	4	OUTMODE	LSB 0x: Analog 1x: Analog and Digital	1	common	
	5		MSB			
	6	(Low)	"0" fixed	0	Y/C	
	7	(Low)	"0" fixed	0		
2	0	DLYH	LSB Delay Adjustment for H1, H2	0h	STG	02h
	1		MSB 0h: +0ns, 1h: +4ns, 2h: +7ns, 3h: –8ns			
	2	DTYH	LSB Duty Adjustment for H1, H2	0h		
	3		MSB 0h: Norm, 1h: F + 3ns, 2h: F + 6ns, 3h: R + 3ns			
	4	DLYRG	LSB Delay Adjustment for RG	0h		
	5		MSB 0h: +0ns, 1h: +4ns, 2h: +7ns, 3h: –8ns			
	6	DTYRG	LSB Duty Adjustment for RG	0h		
	7		MSB 0h: Norm, 1h: F + 3ns, 2h: F + 6ns, 3h: R + 3ns			
3	0	IRLESS	IR less mode 1: ON	0	AWB/MAIN	03h
	1	VIDEOAE	Video AE mode 1: ON	1	AE/MAIN	
	2	ADCKSEL	LSB ADCK Phase Adjustment	0h	STG	
	3		MSB 0h: +0Tck, 1h: +1/4Tck, 2h: +2/4Tck, 3h: +3/4Tck			
	4	(Low)	"0" fixed	0		
	5					
	6	OPBCKINV	Clock Invert for 1st FF after ADC 0: Norm, 1: INV	0	PRE	
	7	(Low)	"0" fixed	0		

#1: Initial setting value with Power-on

CAT1		Serial input				
Byte	bit	Name	Description	#1	Block	Address
4	0	(Low)	"0" fixed	0		04h
	1	(Low)	"0" fixed	0		
	2	(Low)	"0" fixed	0		
	3	(Low)	"0" fixed	0		
	4					
	5	S2DLY	LSB Delay Adjustment for S2 MSB 0h: +0ns, 1h: +15ns, 2h: +30ns, 3h: +45ns	0h	TOP	
	6					
	7	(Low)	"0" fixed	0		
5	0	(Low)	"0" fixed	0		05h
	1					
	2					
	3					
	4					
	5					
	6					
	7	SPINSW	S0, 1, 2 pin active SW 0: Active, 1: Hi-Z	0	TOP	
6	0	ESMODE	Ext Sync mode 0: INT, 1: LL	0	TOP/STG	06h
	1	(Low)	"0" fixed	0		
	2	CMPMODE	P-COMP MODE 0: Norm 1: VCOMP mode (pin release)	0	TOP/STG	
	3	(Low)	"0" fixed	0		
	4	CMPINV	P-COMP ref/var INVerse 0: Normal, 1: Inverse	0	STG	
	5	(Low)	"0" fixed	0		
	6					
	7					
7	0	S0SEL	LSB S0 pin select 0h: FLD, 1h: SYNC, 2h: BF, 3h: DISP MSB 4h: VD, 5h: HD, 6h: CBLK, 7h: DBLK	0h	TOP/STG	07h
	1					
	2					
	3	SSHIFT	Sync SHIFT (shiftVD/HD) 1: Select shiftVD	0	STG	
	4	S1SEL	LSB S1 pin select 00: VD, 01: FLD, 10: HD, 11: DISP MSB ESMODE = LL: S1 = AC in	0h	STG	
	5					
	6	S2SEL	LSB S2 pin select MSB 00: HD, 01: FLD, 10: VD, 11: DISP	0h	STG	
	7					

#1: Initial setting value with Power-on

Category 2: CPU

CAT2		Serial input				
Byte	bit	Name	Description	#1	Block	Address
0	0	CAT2	LSB Category select code 02h: CPU MSB			
	1					
	2					
	3					
	4					
	5					
	6					
	7					
1	0	CPUCMD	LSB CPU Command (EEPROM, AECMD, AWBCMD) MSB	0h	MAIN	
	1					
	2					
	3					
	4					
	5					
	6					
	7					
2	0	CPUADRS	LSB CPU Address MSB	0h	MAIN	
	1					
	2					
	3					
	4					
	5					
	6					
	7					
3	0	CPUDATA	LSB CPU Data MSB	0h	MAIN	
	1					
	2					
	3					
	4					
	5					
	6					
	7					

#1: Initial setting value with Power-on

CAT2		Serial input				
Byte	bit	Name	Description	#1	Block	Address
4	0	CPUEXT	0: CPU, 1: EXT micon mode	0	MAIN	
	1	CPUAE	0: CPU, 1: AE hold (stop)	0		
	2	CPUAWB	0: CPU, 1: AWB hold (stop)	0		
	3	CPUSPRS	0: CPU, 1: SPRS hold (stop)	0		
	4	CPUDIP	0: CPU, 1: Ext Dip SW OFF	0		
	5	CPUSG	0: CPU, 1: SFT UP/DOWN Function OFF	0		
	6	—				
	7					
5	0	NORMFL	Normal FL (AGC + SHT) SW 1: ON	1	MAIN	08h
	1	LIMFL	LIMIT FL SW 1: ON	0		
	2	SFIXFL	Shutter FIX FL Control 1: ON	0		
	3	LAEFL1	Link AE FL1 (NORMFL) Control 1: ON	0		
	4	LAEFL2	Link AE FL2 (LIMFL) Control 1: ON	0		
	5	(Low)	"0" fixed	0		
	6	LAWBFL	Link AWB FL Control 1: ON	0		
	7	(Low)	"0" fixed	0		
6	0	AEME	Auto/Manual Exposure 0: Auto, 1: Normal	0	AE	09h
	1	MIRIS	Mechanical IRIS	0		
	2	BLCOFF	BackLight OFF	0		
	3	AEREF	AE REFerence up	0		
	4	AGCMAX	AGC MAX gain	0		
	5	SHTFIX	Shutter Fix (1/100)	0		
	6	AESHUT	AE Shutter mode	0		
	7	—				
7	0	AWB	LSB AWB mode 0h: ATW, 1h: IN, 2h: PUSH, 3h: USR, 4h: —, 5h: FL, 6h: HOLD, 7h: OUT MSB	0h	AWB	0Ah
	1					
	2					
	3	—				
	4	(Low)	"0" fixed	0		
	5	SFTUP	Shift UP	0	MAIN	
	6	SFTDWN	Shift DOWN	0	MAIN	
	7	—				

#1: Initial setting value with Power-on

CAT2		Serial input				
Byte	bit	Name	Description	#1	Block	Address
8	0	P0CB	LSB Port 0 Cat/Byte MSB	46h	MAIN	0Bh
	1					
	2					
	3					
	4					
	5					
	6					
	7					
9	0	P0M	LSB Port 0 Mode MSB	00h	MAIN	0Ch
	1					
	2					
	3					
	4					
	5					
	6					
	7					
10	0	P1CB	LSB Port 1 Cat/Byte MSB	46h	MAIN	0Dh
	1					
	2					
	3					
	4					
	5					
	6					
	7					
11	0	P1M	LSB Port 1 Mode MSB	01h	MAIN	0Eh
	1					
	2					
	3					
	4					
	5					
	6					
	7					

#1: Initial setting value with Power-on

CAT2		Serial input				
Byte	bit	Name	Description	#1	Block	Address
12	0	P2CB	LSB Port 2 Cat/Byte MSB	46h	MAIN	0Fh
	1					
	2					
	3					
	4					
	5					
	6					
	7					
13	0	P2M	LSB Port 2 Mode MSB	02h	MAIN	10h
	1					
	2					
	3					
	4					
	5					
	6					
	7					
14	0	P3CB	LSB Port 3 Cat/Byte MSB	46h	MAIN	11h
	1					
	2					
	3					
	4					
	5					
	6					
	7					
15	0	P3M	LSB Port 3 Mode MSB	04h	MAIN	12h
	1					
	2					
	3					
	4					
	5					
	6					
	7					

#1: Initial setting value with Power-on

CAT2		Serial input				
Byte	bit	Name	Description	#1	Block	Address
16	0	P4CB	LSB Port 4 Cat/Byte MSB	46h	MAIN	13h
	1					
	2					
	3					
	4					
	5					
	6					
	7					
17	0	P4M	LSB Port 4 Mode MSB	05h	MAIN	14h
	1					
	2					
	3					
	4					
	5					
	6					
	7					
18	0	P5CB	LSB Port 5 Cat/Byte MSB	47h	MAIN	15h
	1					
	2					
	3					
	4					
	5					
	6					
	7					
19	0	P5M	LSB Port 5 Mode MSB	00h	MAIN	16h
	1					
	2					
	3					
	4					
	5					
	6					
	7					

#1: Initial setting value with Power-on

CAT2		Serial input				
Byte	bit	Name	Description	#1	Block	Address
20	0	P6CB	LSB Port 6 Cat/Byte MSB	47h	MAIN	17h
	1					
	2					
	3					
	4					
	5					
	6					
	7					
21	0	P6M	LSB Port 6 Mode MSB	01h	MAIN	18h
	1					
	2					
	3					
	4					
	5					
	6					
	7					
22	0	P7CB	LSB Port 7 Cat/Byte MSB	47h	MAIN	19h
	1					
	2					
	3					
	4					
	5					
	6					
	7					
23	0	P7M	LSB Port 7 Mode MSB	02h	MAIN	1Ah
	1					
	2					
	3					
	4					
	5					
	6					
	7					

#1: Initial setting value with Power-on

Category 3: PICT

CAT3		Serial input				
Byte	bit	Name	Description	#1	Block	Address
0	0	CAT3	LSB Category select code 03h: PICT MSB			
	1					
	2					
	3					
	4					
	5					
	6					
	7					
1	0	HAPGL	LSB H Apcom Gain (Low Freq) MSB	3h	Y	1Bh
	1					
	2	HAPGH	LSB H Apcom Gain (High Freq) MSB	1h		
	3					
	4	YLPFSW	Y-LPF SW (on/off) 1: OFF	0		
	5	(Low)	"0" fixed	0		
	6	GAMSW	Y/C GAMMA SW (on/off) 1: OFF	0	Y/C/MAIN	
	7	—				
2	0	VAPG	LSB V Apcom Gain MSB	Ah	Y	1Ch
	1					
	2					
	3					
	4	VAPSL	LSB V Apcom Slice Level MSB	2h		
	5					
	6					
	7	(Low)	"0" fixed	0		
3	0	VHAPG	LSB VH Apcom Gain MSB	6h	Y	1Dh
	1					
	2					
	3					
	4	VHAPSL	LSB VH Apcom Slice Level MSB	4h		
	5					
	6					
	7					

#1: Initial setting value with Power-on

CAT3		Serial input				
Byte	bit	Name	Description	#1	Block	Address
4	0	ASPRSTA	LSB Apcom SUPPRESS START MSB	A0h	MAIN	1Eh
	1					
	2					
	3					
	4					
	5					
	6					
	7					
5	0	ASPREND	LSB Apcom SUPPRESS END MSB	D0h	MAIN	1Fh
	1					
	2					
	3					
	4					
	5					
	6					
	7					
6	0	ASPRLV	LSB Apcom SUPPRESS LEVEL MSB	00h	MAIN	20h
	1					
	2					
	3					
	4					
	5					
	6					
	7					
7	0	YGAIN	LSB Y GAIN MSB	5Ah	Y	21h
	1					
	2					
	3					
	4					
	5					
	6					
	7					

#1: Initial setting value with Power-on

CAT3		Serial input				
Byte	bit	Name	Description	#1	Block	Address
8	0	SETUP	LSB SETUP level MSB	Dh	Y	22h
	1					
	2					
	3					
	4	WCLIP	LSB White CLIP level MSB	5h		
	5					
	6					
	7	(Low)	"0" fixed	0		
9	0	BSTLV	LSB Burst Level MSB	NT = 12h PAL = 13h	DENC	23h
	1					
	2					
	3					
	4					
	5	BSTINV	Burst Inverse 0: Inverse, 1: Normal	1		
	6	(Low)	"0" fixed	0		
	7	MIRROR	Mirror SW 0: Normal, 1: Mirror	0	Y/C	
10	0	RYGAIN	LSB R-Y Gain MSB	2Fh	C	24h
	1					
	2					
	3					
	4					
	5					
	6					
	7					
11	0	BYGAIN	LSB B-Y Gain MSB	1Ch	C	25h
	1					
	2					
	3					
	4					
	5					
	6					
	7					

#1: Initial setting value with Power-on

CAT3		Serial input				
Byte	bit	Name	Description	#1	Block	Address
12	0	RYHUE	LSB R-Y HUE MSB	FFh	C	26h
	1					
	2					
	3					
	4					
	5					
	6					
	7					
13	0	BYHUE	LSB B-Y HUE MSB	FEh	C	27h
	1					
	2					
	3					
	4					
	5					
	6					
	7					
14	0	CSPRSTA	LSB C SUPPRESS START MSB	A0h	MAIN	28h
	1					
	2					
	3					
	4					
	5					
	6					
	7					
15	0	CSPREND	LSB C SUPPRESS END MSB	D0h	MAIN	29h
	1					
	2					
	3					
	4					
	5					
	6					
	7					

#1: Initial setting value with Power-on

CAT3		Serial input				
Byte	bit	Name	Description	#1	Block	Address
16	0	CSPRLV	LSB C SUPPRESS LEVEL MSB	8Ah	MAIN	2Ah
	1					
	2					
	3					
	4					
	5					
	6					
	7					
17	0	CSVLV	LSB C Suppress V apcom Level MSB	0h	C	2Bh
	1					
	2	CSVTH	LSB C Suppress V apcom THreshold MSB	1h	Y	
	3					
	4	CSHLV	LSB C Suppress Highlight Level MSB	0h	C	
	5					
	6	CSHTH	LSB C Suppress Highlight Threshold MSB	2h	Y	
	7					
18	0	YSPRLV	LSB Y Suppress Highlight Level MSB	0h	Y/(C)	2Ch
	1					
	2	YSPRTH	LSB Y Suppress Highlight Threshold MSB	0h	Y/(C)	
	3					
	4	HLLIM	LSB Highlight LIMiter level MSB	0h	DENC	
	5					
	6	PEDLIM	LSB PEDestal LIMiter level MSB	0h	DENC	
	7					
19	0	GOFGAIN	LSB Gamma OFF Y/C GAIN MSB	00h	MAIN	2Dh
	1					
	2					
	3					
	4					
	5					
	6					
	7					

#1: Initial setting value with Power-on

Category 4: AE

CAT4		Serial input				
Byte	bit	Name	Description	#1	Block	Address
0	0	CAT4	LSB Category select code 04h: AE MSB			
	1					
	2					
	3					
	4					
	5					
	6					
	7					
1	0	AEW0	LSB AE Wind0 weight MSB	0h	OPD	2Fh
	1					
	2	AEW1	LSB AE Wind1 weight MSB	0h		
	3					
	4	AEW2	LSB AE Wind2 weight MSB	0h		
	5					
	6	AEW3	LSB AE Wind3 weight MSB	0h		
	7					
2	0	AGCFL	AGC FL	0	AE	30h
	1	SHTFL	Shutter FL	0		
	2	LSHTLIM	Low speed Shut Lim 0: Normal, 1: Limit ON	0		
	3	(Low)	"0" fixed	0		
	4	EVR5V	EVR voltage select 0: 3.3V, 1: 5V	0		
	5	—				
	6					
	7	(Low)	"0" fixed	0		
3	0	AESTAB	LSB AE Stability MSB	0h	AE	31h
	1					
	2					
	3					
	4					
	5					
	6					
	7					

#1: Initial setting value with Power-on

CAT4		Serial input				
Byte	bit	Name	Description	#1	Block	Address
4	0	AEHYST	LSB AE HYSTeresis MSB	0h	AE	32h
	1					
	2					
	3					
	4					
	5					
	6					
	7					
5	0	AEWAIT	LSB AE WAIT counter MSB	0h	AE	33h
	1					
	2					
	3					
	4					
	5					
	6					
	7					
6	0	AESPEED	LSB AE SPEED MSB	08h	AE	34h
	1					
	2					
	3					
	4					
	5					
	6					
	7					
7	0	AEUSR	LSB AE USR setting level MSB	04h	AE	35h
	1					
	2					
	3					
	4					
	5					
	6					
	7					

#1: Initial setting value with Power-on

CAT4		Serial input				
Byte	bit	Name	Description	#1	Block	Address
8	0	AGCMAXL	LSB AE AGC MAX Low (AGCMAX = 0) MSB	CCh	AE	36h
	1					
	2					
	3					
	4					
	5					
	6					
	7					
9	0	AGCMAXH	LSB AE AGC MAX High (AGCMAX = 1) MSB	FFh	AE	37h
	1					
	2					
	3					
	4					
	5					
	6					
	7					
10	0	MSHTLIM	LSB AE MAX speed shut Lim MSB	7h	AE	38h
	1					
	2					
	3					
	4					
	5					
	6					
	7					
11	0	AGCFLLL	LSB AE AGC FL lower Lim MSB	20h	AE	39h
	1					
	2					
	3					
	4					
	5					
	6					
	7					

#1: Initial setting value with Power-on

CAT4		Serial input				
Byte	bit	Name	Description	#1	Block	Address
12	0	SHTFLLL	LSB AE SHUTTER FL Lower Lim MSB	1h	AE	3Ah
	1					
	2					
	3					
	4	SHTFLUL	LSB AE SHUTTER FL Upper Lim MSB	Bh		
	5					
	6					
	7					
13	0	AETHL	LSB AE THRESHOLD Low MSB	10h	AE	3Bh
	1					
	2					
	3					
	4					
	5					
	6					
	7					
14	0	AETHH	LSB AE THRESHOLD High MSB	20h	AE	3Ch
	1					
	2					
	3					
	4					
	5					
	6					
	7					

#1: Initial setting value with Power-on

Category 5: AWB

CAT5		Serial input				
Byte	bit	Name	Description	#1	Block	Address
0	0	CAT5	LSB Category select code 05h: AWB MSB			
	1					
	2					
	3					
	4					
	5					
	6					
	7					
1	0	AWBW0	LSB AWB Wind0 weight MSB	0h	OPD	3Dh
	1					
	2	AWBW1	LSB AWB Wind1 weight MSB	0h		
	3					
	4	AWBW2	LSB AWB Wind2 weight MSB	0h		
	5					
	6	AWBW3	LSB AWB Wind3 weight MSB	0h		
	7					
2	0	AWBSEPOF	AWB light SEParate OFF	0h	AWB	3Eh
	1	AWBTRIG	AWB TRIGger ON/OFF	0h		
	2	AWBHLCUT	LSB AWB High Light CUT block MSB	0h		
	3					
	4	AWBLLCUT	AWB Low Light integ data CUT	0h		
	5	—				
	6					
	7					
3	0	GGAIN	LSB Green GAIN (push lock mode) MSB	26h	AWB	3Fh
	1					
	2					
	3					
	4					
	5					
	6					
	7					

#1: Initial setting value with Power-on

CAT5		Serial input				
Byte	bit	Name	Description	#1	Block	Address
4	0 1 2 3 4 5 6 7	—				
5	0 1 2 3	AWBSPED	LSB AWB SPEED (0: PUSH mode) MSB	1h	AWB	41h
	4 5	AWBAJST5	LSB AWB Adjust5 MSB	0h		
	6 7	AWBAJST6	LSB AWB Adjust6 MSB	0h		
6	0 1 2 3 4 5 6 7	AWBFRAM	LSB AWB vector FRAME MSB	00h	AWB	42h
7	0 1 2 3 4 5 6 7	AWBRSFT	LSB AWB ATW R shift MSB	00h	AWB	43h

#1: Initial setting value with Power-on

CAT5		Serial input				
Byte	bit	Name	Description	#1	Block	Address
8	0	AWBBSFT	LSB AWB ATW B shift MSB	00h	AWB	44h
	1					
	2					
	3					
	4					
	5					
	6					
	7					
9	0	—				
	1					
	2					
	3					
	4					
	5					
	6					
	7					
10	0	—				
	1					
	2					
	3					
	4					
	5					
	6					
	7					
11	0	WBUSRR	LSB AWB USR mode R gain MSB	49h	AWB	47h
	1					
	2					
	3					
	4					
	5					
	6					
	7					

#1: Initial setting value with Power-on

CAT5		Serial input				
Byte	bit	Name	Description	#1	Block	Address
12	0	WBUSRB	LSB AWB USR mode B gain MSB	2Ch	AWB	48h
	1					
	2					
	3					
	4					
	5					
	6					
	7					
13	0	WBRSFT	LSB WB R shift MSB	3h	AWB	49h
	1					
	2					
	3					
	4					
	5					
	6					
	7					
14	0	WBBSFT	LSB WB B shift MSB	1h	AWB	4Ah
	1					
	2					
	3					
	4					
	5					
	6					
	7					

#1: Initial setting value with Power-on

Category 6: ADJUST

CAT6		Serial input				
Byte	bit	Name	Description	#1	Block	Address
0	0	CAT6	LSB Category select code 06h: ADJUST MSB			
	1					
	2					
	3					
	4					
	5					
	6					
	7					
1	0	VSUB	LSB CCD: VSUB MSB	00h	EVR3	4Bh
	1					
	2					
	3					
	4					
	5					
	6					
	7					
2	0	RGL	LSB CCD: RGL MSB	00h	EVR4	4Ch
	1					
	2					
	3					
	4					
	5					
	6					
	7					
3	0	AGCMIN	LSB S/H: AGC MIN gain MSB	11h	AE	4Dh
	1					
	2					
	3					
	4					
	5					
	6					
	7					

#1: Initial setting value with Power-on

CAT6		Serial input				
Byte	bit	Name	Description	#1	Block	Address
4	0	SHOFST	LSB S/H: OFFSET MSB	A0h	EVR5	4Eh
	1					
	2					
	3					
	4					
	5					
	6					
	7					
5	0	DAVRF	LSB D/A: VREF MSB	58h	EVR6	4Fh
	1					
	2					
	3					
	4					
	5					
	6					
	7					
6	0	EVRUSR7	LSB User setting EVR7 MSB	00h	EVR7	50h
	1					
	2					
	3					
	4					
	5					
	6					
	7					
7	0	EVRUSR8	LSB User setting EVR8 MSB	00h	EVR8	51h
	1					
	2					
	3					
	4					
	5					
	6					
	7					

#1: Initial setting value with Power-on

CAT6		Serial input				
Byte	bit	Name	Description	#1	Block	Address
8	0	AWBPRER	LSB PRE white balance R MSB	37h	AWB	52h
	1					
	2					
	3					
	4					
	5					
	6					
	7					
9	0	AWBPREB	LSB PRE white balance B MSB	39h	AWB	53h
	1					
	2					
	3					
	4					
	5					
	6					
	7					
10	0	PRERBL	LSB PRE R-B L MSB	00h	AWB	54h
	1					
	2					
	3					
	4					
	5					
	6					
	7					
11	0	PRERBH	LSB PRE R-B H MSB	0Ah	AWB	55h
	1					
	2					
	3					
	4					
	5					
	6					
	7					

#1: Initial setting value with Power-on

CAT6		Serial input				
Byte	bit	Name	Description	#1	Block	Address
12	0	PRERBGL	LSB PRE R + B – 2G L MSB	00h	AWB	56h
	1					
	2					
	3					
	4					
	5					
	6					
	7					
13	0	PRERBGH	LSB PRE R + B – 2G H MSB	23h	AWB	57h
	1					
	2					
	3					
	4					
	5					
	6					
	7					
14	0	PRE2R	LSB AWB PRE WB2 R MSB	60h	AWB	58h
	1					
	2					
	3					
	4					
	5					
	6					
	7					
15	0	PRE2B	LSB AWB PRE WB2 B MSB	20h	AWB	59h
	1					
	2					
	3					
	4					
	5					
	6					
	7					

#1: Initial setting value with Power-on

CAT6		Serial input				
Byte	bit	Name	Description	#1	Block	Address
16	0	AWBAJST1	LSB AWB Adjust1 MSB	18h	AWB	5Ah
	1					
	2					
	3					
	4					
	5					
	6					
	7					
17	0	AWBAJST2	LSB AWB Adjust2 MSB	1Ch	AWB	5Bh
	1					
	2					
	3					
	4					
	5					
	6					
	7					
18	0	AWBAJST3	LSB AWB Adjust3 MSB	00h	AWB	5Ch
	1					
	2					
	3					
	4					
	5					
	6					
	7					
19	0	AWBAJST4	LSB AWB Adjust4 MSB	00h	AWB	5Dh
	1					
	2					
	3					
	4					
	5					
	6					
	7					

#1: Initial setting value with Power-on

CAT6		Serial input				
Byte	bit	Name	Description	#1	Block	Address
20	0	BLOGAIN	LSB B LOW GAIN MSB	46h	AWB	5Eh
	1					
	2					
	3					
	4					
	5					
	6					
	7					
21	0	INTSLICE	LSB INTEG SLICE level MSB	80h	AWB	5Fh
	1					
	2					
	3					
	4					
	5					
	6					
	7					

#1: Initial setting value with Power-on

Category 7: TIMING

CAT7		Serial input					
Byte	bit	Name	Description		#1	Block	Address
0	0	CAT7	LSB Category select code 07h: TIMING MSB				
	1						
	2						
	3						
	4						
	5						
	6						
	7						
1	0	WINDSEL	LSB WIND/DISP SELect MSB		3h	OPD	61h
	1						
	2	WINDMK	WIND MarKer on	1: ON	0	Y	
	3	DEFMK	DEFect 1, 2 MarKer on	1: ON	0	DLY	
	4	SVHMK	SHIFT VD MarKer on	1: ON	0	Y	
	5	—					
	6						
	7						
2	0	W3STAH	LSB Wind3 H START MSB		5h	STG	62h
	1						
	2						
	3						
	4	W3WIDH	LSB Wind3 H WIDTH MSB		5h		
	5						
	6						
	7						
3	0	W3STAV	LSB Wind3 V START MSB		4h	STG	63h
	1						
	2						
	3						
	4	W3WIDV	LSB Wind3 V WIDTH MSB		7h		
	5						
	6						
	7						

#1: Initial setting value with Power-on

CAT7		Serial input				
Byte	bit	Name	Description	#1	Block	Address
4	0	(Low)	"0" fixed	0		64h
	1					
	2					
	3					
	4	ADCKDLY	LSB Delay Adjustment for ADCK MSB	2h	STG	
	5					
	6	(Low)	"0" fixed	0		
	7	OFFSET25	PAL 25Hz Offset 0: Normal, 1: 25Hz Offset	0	DENC	
5	0	DLYXSH	LSB Delay Adjustment for XSHP, XSHD MSB 0h: 0ns, 1h: +4ns, 2h: +7ns, 3h: –8ns	0h	STG	65h
	1					
	2	DTYXSH	LSB Duty Adjustment for XSHP, XSHD MSB 0h: Norm, 1h: F + 3ns, 2h: F + 6ns, 3h: R + 3ns	0h		
	3					
	4	DLYXRS	LSB Delay Adjustment for XRS MSB 0h: 0ns, 1h: +4ns, 2h: +7ns, 3h: –8ns	0h		
	5					
	6	DTYXRS	LSB Duty Adjustment for XRS MSB 0h: Norm, 1h: F + 3ns, 2h: F + 6ns, 3h: R + 3ns	0h		
	7					
6	0	(Low)	"0" fixed	0		66h
	1					
	2					
	3					
	4					
	5					
	6					
	7					
7	0	(Low)	"0" fixed	0		
	1					
	2	—				
	3					
	4	(Constant)	"2"h fixed	2h		
	5					
	6					
	7	—				

#1: Initial setting value with Power-on

CAT7		Serial input				
Byte	bit	Name	Description	#1	Block	Address
8	0	(Low)	"0" fixed	0		68h
	1					
	2					
	3					
	4					
	5					
	6					
	7					
9	0	SFTVL	LSB SHIFTER V Lsb 8 bit	01h	STG	69h
	1					
	2					
	3					
	4					
	5					
	6					
	7		MSB			
10	0	(Low)	"0" fixed	0		6Ah
	1					
	2	SFTVM	SHIFTER V Msb 1 bit	0h	STG	
	3	(Low)	"0" fixed	0		
	4	SFTSPED	LSB	0h	MAIN	
	5		SHIFTER SPEED Adjustment			
	6		MSB			
	7	(Constant)	"1" fixed	1		
11	0	DEF1HL	LSB DEFect 1 H Lsb 8 bit	0h	STG	6Bh
	1					
	2					
	3					
	4					
	5					
	6					
	7		MSB			

#1: Initial setting value with Power-on

CAT7		Serial input				
Byte	bit	Name	Description	#1	Block	Address
12	0	DEF1VL	LSB DEFect 1 V Lsb 8 bit MSB	0h	STG	6Ch
	1					
	2					
	3					
	4					
	5					
	6					
	7					
13	0	DEF1HM	LSB DEFect 1 H Msb 2 bit MSB	0h	STG	2Eh
	1					
	2	DEF1VM	LSB DEFect 1 V Msb 2 bit MSB	0h	STG	
	3					
	4	DEF1L	DEFect 1 Large def	0	STG	
	5	—				
	6					
	7					
14	0	DEF2HL	LSB DEFect 2 H Lsb 8 bit MSB	0h	STG	6Eh
	1					
	2					
	3					
	4					
	5					
	6					
	7					
15	0	DEF2VL	LSB DEFect 2 V Lsb 8 bit MSB	0h	STG	6Fh
	1					
	2					
	3					
	4					
	5					
	6					
	7					

#1: Initial setting value with Power-on

CAT7		Serial input				
Byte	bit	Name	Description	#1	Block	Address
16	0	DEF2HM	LSB MSB DEFect 2 H Msb 2 bit	0h	STG	60h
	1					
	2	DEF2VM	LSB MSB DEFect 2 V Msb 2 bit	0h	STG	
	3					
	4	DEF2L	DEFect 2 Large def	0	STG	
	5	—				
	6					
	7					

#1: Initial setting value with Power-on

Category 8: SOUT

CAT8		Serial input				
Byte	bit	Name	Description	#1	Block	Address
0	0	CAT8	LSB			
	1					
	2					
	3		Category select code 08h: SOUT			
	4					
	5					
	6					
	7		MSB			
1	0	SOBYTE	LSB	00h	MAIN	
	1					
	2					
	3		Serial Out start Byte number			
	4					
	5					
	6					
	7		MSB			

#1: Initial setting value with Power-on

Category 9: EXTCON

CAT9		Serial input				
Byte	bit	Name	Description	#1	Block	Address
0	0	CAT9	LSB Category select code 09h: EXTCON MSB			
	1					
	2					
	3					
	4					
	5					
	6					
	7					
1	0	—				
	1					
	2					
	3					
	4					
	5					
	6					
	7					
2	0	—				
	1					
	2					
	3					
	4					
	5					
	6					
	7					
3	0	—				
	1					
	2					
	3					
	4					
	5					
	6					
	7					

#1: Initial setting value with Power-on

CAT9		Serial input				
Byte	bit	Name	Description	#1	Block	Address
4	0 1 2 3 4 5 6 7	—				
5	0 1 2 3 4 5 6 7	WBR	LSB WB R gain MSB	37h	C	
6	0 1 2 3 4 5 6 7	WBG	LSB WB G gain MSB	26h	C	
7	0 1 2 3 4 5 6 7	WBB	LSB WB B gain MSB	39h	C	

#1: Initial setting value with Power-on

CAT9		Serial input				
Byte	bit	Name	Description	#1	Block	Address
8	0	WBYREFH	LSB Y slice High Level MSB	D0h	OPD	
	1					
	2					
	3					
	4					
	5					
	6					
	7					
9	0	WBYREFL	LSB Y slice Low Level MSB	04h	OPD	
	1					
	2					
	3					
	4					
	5					
	6					
	7					
10	0	(Low)	"00"h fixed	00h		
	1					
	2					
	3					
	4					
	5					
	6					
	7					
11	0	(Low)	"00"h fixed	00h		
	1					
	2					
	3					
	4					
	5					
	6					
	7					

#1: Initial setting value with Power-on

CAT9		Serial input				
Byte	bit	Name	Description	#1	Block	Address
12	0	—				72h
	1					
	2					
	3					
	4	DRSL1	LSB H-driver ability (H1, H2)	1h	TOP	
	5					
	6		MSB			
	7	—				
13	0	(Low)	"0" fixed	0		73h
	1					
	2	(Constant)	"3"h fixed	3h		
	3					
	4	(Constant)	"1"h fixed	1h		
	5	(Low)	"0" fixed	0		
	6					
	7	IDINV	ID INVerse	NT = 0h PAL = 1h	C	
14	0	(Low)	LSB "0" fixed	0		74h
	1					
	2					
	3		MSB			
	4	PLLSW	PLLSW 0: Normal, 1: ON (38MHz)	0	TOP	
	5	DRSL2	LSB H-driver ability (RG)	1h	TOP	
	6					
	7		MSB			
15	0	YDLY	LSB Y DLY 0 – 3CK	0h	Y	75h
	1		MSB			
	2	CDLY	LSB C DLY 0 – 3CK	0h	C	
	3		MSB			
	4	YDDLY	LSB Y Digital DLY 0 – 3CK	0h	DIF	
	5		MSB			
	6	CDDLY	LSB C Digital DLY 0 – 3CK	0h	DIF	
	7		MSB			

#1: Initial setting value with Power-on

CAT9		Serial input				
Byte	bit	Name	Description	#1	Block	Address
16	0	RMATY	LSB R matrix R = RMATY × Yr + Cr + RMATC × Cb MSB	2Dh	C	76h
	1					
	2					
	3					
	4					
	5					
	6					
	7					
17	0	RMATC	LSB R matrix R = RMATY × Yr + Cr + RMATC × Cb MSB	00h	C	77h
	1					
	2					
	3					
	4					
	5					
	6					
	7					
18	0	BMATY	LSB B matrix B = BMATY × Yb + Cb + BMATC × Cr MSB	45h	C	78h
	1					
	2					
	3					
	4					
	5					
	6					
	7					
19	0	BMATC	LSB B matrix B = BMATY × Yb + Cb + BMATC × Cr MSB	BBh	C	79h
	1					
	2					
	3					
	4					
	5					
	6					
	7					

#1: Initial setting value with Power-on

CAT9		Serial input				
Byte	bit	Name	Description	#1	Block	Address
20	0	(Low)	"0" fixed	0		7Ah
	1					
	2	DRSL3	LSB H-driver ability (XSHP, XSHD) MSB	1h	TOP	
	3					
	4					
	5	DRSL4	LSB H-driver ability (XRS) MSB	1h	TOP	
	6					
	7					

#1: Initial setting value with Power-on

Serial output

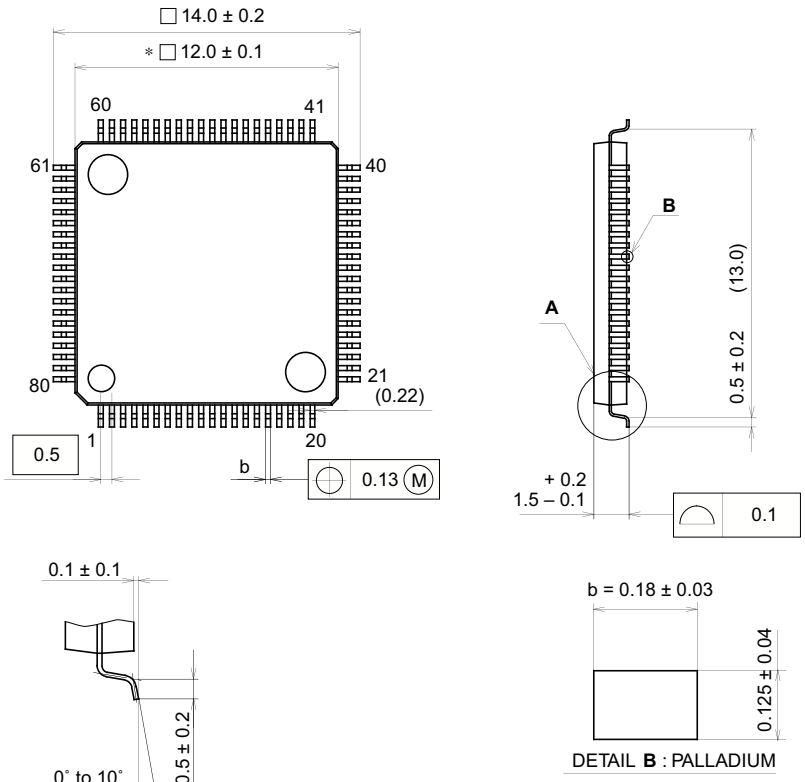
CAT8		Serial output		
Byte	bit	Name	Description	Block
1	0	—		
	1			
	2			
	3			
	4			
	5			
	6			
	7			
2	0	—		
	1			
	2			
	3			
	4			
	5			
	6			
	7			
3	0	—		
	1			
	2			
	3			
	4			
	5			
	6			
	7			
4	0	—		
	1			
	2			
	3			
	4			
	5			
	6			
	7			

CAT8		Serial output		
Byte	bit	Name	Description	Block
5	0	AWOUT1	LSB AWB OUT 1 MSB	AWB
	1			
	2			
	3			
	4			
	5			
	6			
	7			
6	0	AWOUT2	LSB AWB OUT 2 MSB	AWB
	1			
	2			
	3			
	4			
	5			
	6			
	7			
7	0	AWOUT3	LSB AWB OUT 3 MSB	AWB
	1			
	2			
	3			
	4			
	5			
	6			
	7			
8	0	AWOUT4	LSB AWB OUT 4 MSB	AWB
	1			
	2			
	3			
	4			
	5			
	6			
	7			

CAT8		Serial output		
Byte	bit	Name	Description	Block
9	0	E2RDATA	LSB EEPROM READ DATA MSB	MAIN
	1			
	2			
	3			
	4			
	5			
	6			
	7			

Package Outline Unit: mm

80PIN LQFP (PLASTIC)



NOTE: Dimension "*" does not include mold protrusion.

DETAIL **A**

SONY CODE	LQFP-80P-L01
EIAJ CODE	P-LQFP80-12x12-0.5
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.5g